REMARKS

Review and reconsideration on the merits are requested.

Formalities

Applicants appreciate the Examiner acknowledging receipt of the certified copy of the priority document; and

Returning PTO/SB/08 dated February 18, 2004.

The Newly Added Claims

Newly added claims 15-21 are product-by-process claims which correspond to process claims 8-14 as filed, respectively, which, it is submitted, quite clearly distinguish the **products** of the present claims from the **products** of Nakayama.

PRIOR ART

U.S. Publication No. 2005/0145879 A1 Nakayama et al (Nakayama).

The Rejection:

Claims 1-7 are rejected under 35 U.S.C. § 102(e) as anticipated by Nakayama. Claims 8-14 are withdrawn.

The rejection of claims 1-7 is respectfully traversed.

The Examiner's reading and application of the prior art are set forth in the Action, and will not be repeated here except as necessary to understand Applicant's traversal which is now presented.

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Traversal

As described in the specification at pages 3/4, the present invention was reached based on the findings that:

(a) the level of the large-area defects in crystals, such as impurities, nitrogen dissociation, polycrystals, voids, etc., can be determined by the mass density of a crystal or its distribution and a high-quality nitride semiconductor crystal with few defects can be obtained by increasing its mass density as an index to a desired level or more;

(b) a high mass density can be obtained by growing a nitride semiconductor with the partial pressure of a nitrogen growth compound gas being kept sufficiently high; and

(c) a heat treatment in a nitrogen compound gas atmosphere after the growth of the nitride semiconductor can further increase the mass density of the nitride semiconductor (see page 3, line 19 to page 4, line 9 of the specification).

At this point, the Examiner is respectfully requested to refer to claim 1 of the present application; following the limits of claim 1, one obtains a high quality nitride semiconductor substrate with reduced defect density, (see page 1, lines 5-7 of the specification), making it possible to produce devices from such a substrate, such as LDs, etc., having high reliability (see page 7, lines 12-18 of the specification).

Major distinguishing features of the claimed invention are found in the following:

(1) a nitride semiconductor substrate having a diameter of 10 mm or more has a single-layer structure composed of a nitride semiconductor layer having a basic composition

represented by $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$), or a multi-layer structure comprising the nitride semiconductor layer; and

(2) the mass density of the nitride semiconductor layer is 98% or more of the theoretical mass density $\rho(x)$.

Applicant respectfully submits that barring any explicit or implicit teaching in Nakayama regarding mass density, Nakayama cannot serve as a proper basis to reject the claims of the present application as anticipated.

Claim 1 specifically recites that the "mass density of said nitride semiconductor layer being 98% or more of a theoretical mass density $\rho(x)$ represented by" general formula (1). Barring some suggestion in Nakayama that mass density is a factor appreciated by Nakayama, Applicant respectfully submits that the anticipation rejection is *per se* improper and should be withdrawn.

However, there are additional reasons why the anticipation rejection over Nakayama is improper, as now explained.

In contrast to the claimed invention, Nakayama discloses a nitride semiconductor wafer having a diameter larger than 45 mm; a single-mode distortion which has a maximum or minimum central height H less than 12 μm (1200 nm) or a distortion curvature radius R longer than 21 m, a top surface of roughness satisfying 0.1 nm ≤ RMS ≤ 5 nm; and a bottom surface of roughness satisfying 0.1 nm ≤ 5000 nm (see claim 1 of Nakayama).

Nakayama is essentially a "polishing" patent, and, for the reasons now advanced, Applicant submits does not suggest the limits of the claims herein.

Although Nakayama teaches a nitride semiconductor layer (wafer) composed of single crystal (see paragraph [0050] of Nakayama) as the Examiner has indicated, Nakayama does not teach or suggest any mass density for the nitride semiconductor layer.

The Examiner is respectfully requested to refer to major distinguishing feature (2) above, namely, that the mass density of the nitride semiconductor layer is 98% or more of the theoretical mass density $\rho(x)$. This major distinguishing feature of the claims herein is **not automatically satisfied** by all GaN single crystal substrates. In fact, GaN single crystal substrates have various mass densities, which, of course, would include mass densities falling **outside** the mass density of the nitride semiconductor layer claimed herein. For instance, the Examiner is requested to refer to Comparative Example 1 in the present specification. In Comparative Example 1, about 97% of the theoretical mass density $\rho(x)$ of the GaN single crystal substrate is obtained by an HVPE method; see page 15, lines 16-27 of the present specification.

The results in Comparative Example 1 reflect the important fact that the mass density of a nitride semiconductor substrate is dependent on the method used to produce the nitride semiconductor substrate *per se*. Example 1 and Example 2 in the present specification specifically describe a method for producing a nitride semiconductor substrate having a single-layer structure composed of a nitride semiconductor layer where the mass density of the nitride semiconductor layer is 98% or more of the theoretical mass density $\rho(x)$. See page 13 to page 15 of the specification.

In this regard, with respect to methods for producing a GaN single crystal substrate, Nakayama at best discloses a general HVPE method, and, basically, Nakayama is silent regarding the production conditions for the Nakayama HVPE method in any substantial detail. Accordingly, Applicant finds himself in a position where it is very unclear as to whether or not the Nakayama method could in any fashion provide a GaN single crystal substrate having a single-layer structure composed of a nitride semiconductor layer where the mass density of the nitride semiconductor layer is 98% or more of the theoretical mass density $\rho(x)$.

In this regard, it is believed that Comparative Example 1 herein is relevant and warrants further discussion. If the Examiner will refer to Comparative Example 1 which is presented beginning at page 15 of the specification, the Examiner will see that a GaN single crystal substrate having an about 97% theoretical mass density $\rho(x)$ was produced by using an MOVPE method, which Applicant believes can generically be considered a HVPE method. Certainly Comparative Example 1 supports the conclusion that it is uncertain whether or not a GaN single crystal substrate produced by HVPE will have a single-layer structure composed of a nitride semiconductor layer or a multi-layer structure comprising a nitride semiconductor layer where the mass density of the nitride semiconductor layer is 98% or more of the theoretical mass density $\rho(x)$.

For the reasons advanced, Applicant submits that the claims herein are not anticipated by Nakayama, or rendered obvious by Nakayama, and for the reasons advanced with respect to claim 1, claims 2-7 of the present application are not anticipated by or rendered obvious by Nakayama.

While the Examiner urges with respect to claims 4, 5 and 7 that these characteristics are "believed to be inherent characteristics of the nitride semiconductor layer disclosed by Nakayama", the Examiner has advanced **no basis** to support the conclusion that such characteristics would **in fact** be posed by the nitride semiconductor layer of Nakayama.

It is well settled that to support an anticipation rejection based on grounds of inherency **some basis** must be advanced for the conclusion of inherency. What is lacking in the present Action is any basis to support the fact that claims 4, 5 and 7 represent mere inherent characteristics of Nakayama.

In this regard, *Ex parte* Skinner, 2 USPQ2d 1788 (Bd. Pat. App. & Int. 1986) is relevant.

Although dealing with claims directed to a mold of the type used to produce plastic articles, the Board had the following comments on an anticipation rejection where the Examiner found that the properties of the mold surface may be inherent characteristics of the reference coating.

> It is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office. *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) quoting *In re Warner*, 379 F.2d 1011, 1016 154 USPQ 173, 177 (CCPA 1967). It is the Examiner's position that the mold of Mizutani may inherently have the characteristics of the claimed mold. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. *In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323 (CCPA 1981). We are mindful that there is a line of cases represented by *In re Swinehart*, 439 F.2d 210, 169 USPQ 226 (CCPA 1971) which indicates that where an Examiner has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, the Examiner possesses the authority to require an applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on. Nevertheless, before an applicant can be put to this burdensome task, the Examiner must provide some evidence or

> scientific reasoning to establish the reasonableness of the Examiner's belief that the functional limitation is an inherent characteristic of the prior art. In the case before us, no such evidence or reasoning has been set forward.

This similar effect is *Ex parte Schricker*, 56 USPQ2d 1723 (Bd. Pat. App. & Int. 2000), unpublished, which is relevant for the following discussion of the Board regarding inherency rejections:

> Inherency and obviousness are somewhat like oil and water - they do not mix well. Claimed subject matter can be anticipated because a prior art reference describes a method which inherently meets the limitations of a claimed method. Claimed subject matter can be unpatentable for obviousness when, notwithstanding a difference between that subject matter and a prior art reference, the claimed subject matter, as a whole, would have been obvious. **However, when an Examiner relies on inherency, it is incumbent on the Examiner to point to the "page and line" of the prior art which justifies an inherency theory.** Compare *In re Rijckaert*, 9 F.3d 1531, 1533, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (when the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the prior art) (citing *In re Yates*, 663 F.2d 1054, 1057, 211 USPQ 1149, 1151 (CCPA 1981)". (bolding added by the undersigned).

Applicants respectfully submit that in the present rejection, the Examiner has not carried his burden of proof, and respectfully request withdrawal of the rejection.

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The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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